

1 CLAIMS:

2 1. A semiconductor memory device comprising:

3 a semiconductor die encapsulated in a package, the package
4 having an encapsulating body and electrically conductive interconnect pins
5 extending outwardly from the body;

6 a total of no more than 68,000,000 functional and operably
7 addressable memory cells arranged in multiple memory arrays formed on
8 the die, the individual functional and operably addressable memory cells
9 occupying area on the die within the memory arrays, the occupied area
10 of all functional and addressable memory cells on the die having a total
11 combined area which is no greater than 53 mm²; and

12 peripheral circuitry and pitch circuitry formed on the die relative
13 to the memory arrays; the peripheral circuitry electrically interconnecting
14 with the pins and including operably interconnected control and timing
15 circuitry, address and redundancy circuitry, data and test path circuitry,
16 and voltage supply circuitry which collectively enable full access to all
17 addressable memory cells of the memory arrays.

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19 2. The semiconductor memory device of claim 1 wherein the
20 die is fabricated to include a total of four or less composite conductive
21 line layers.

1 3. The semiconductor memory device of claim 1 wherein the
2 peripheral circuitry, the pitch circuitry and the memory arrays have a
3 total combined continuous surface area on the die which is less than
4 or equal to 106 mm^2 .

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6 4. The semiconductor memory device of claim 1 wherein the
7 peripheral circuitry, the pitch circuitry, and the memory arrays are
8 fabricated to include at least five composite conductive line layers, the
9 occupied area of all functional and operable memory cells on the die
10 having a total combined area on the die which is no greater than
11 40 mm^2 .

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13 5. The semiconductor memory device of claim 1 wherein the
14 peripheral circuitry, the pitch circuitry, and the memory arrays are
15 fabricated to include at least five composite conductive line layers; the
16 peripheral circuitry, the pitch circuitry and the memory arrays having a
17 total combined continuous surface area on the die which is less than
18 or equal to 93 mm^2 .

1 6. A semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package
3 having an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;
5 a total of no more than 17,000,000 functional and operably
6 addressable memory cells arranged in multiple memory arrays formed on
7 the die, the individual functional and operably addressable memory cells
8 occupying area on the die within the memory arrays, the occupied area
9 of all functional and addressable memory cells on the die having a total
10 combined area which is no greater than 14 mm²; and
11 peripheral circuitry and pitch circuitry formed on the die relative
12 to the memory arrays; the peripheral circuitry electrically interconnecting
13 with the pins and including operably interconnected control and timing
14 circuitry, address and redundancy circuitry, data and test path circuitry,
15 and voltage supply circuitry which collectively enable full access to all
16 addressable memory cells of the memory arrays.
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18 7. The semiconductor memory device of claim 6 wherein the
19 peripheral circuitry, the pitch circuitry, and the memory arrays are
20 fabricated to include a total of four or less composite conductive line
21 layers.
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1 8. The semiconductor memory device of claim 6 wherein the
2 peripheral circuitry, the pitch circuitry and the memory arrays have a
3 total combined continuous surface area on the die which is less than
4 or equal to 35 mm².

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6 9. The semiconductor memory device of claim 6 wherein the
7 peripheral circuitry, the pitch circuitry, and the memory arrays are
8 fabricated to include at least five composite conductive line layers, the
9 occupied area of all functional and operable memory cells on the die
10 having a total combined area on the die which is no greater than
11 11 mm².

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13 10. The semiconductor memory device of claim 6 wherein the
14 peripheral circuitry, the pitch circuitry, and the memory arrays are
15 fabricated to include at least five composite conductive line layers; the
16 peripheral circuitry, the pitch circuitry and the memory arrays having a
17 total combined continuous surface area on the die which is less than
18 or equal to 32 mm².

1 11. A semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package
3 having an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;
5 a total of no more than 4,500,000 functional and operably
6 addressable memory cells arranged in multiple memory arrays formed on
7 the die, the individual functional and operably addressable memory cells
8 occupying area on the die within the memory arrays, the occupied area
9 of all functional and addressable memory cells on the die having a total
10 combined area which is no greater than 3.3 mm^2 ; and
11 peripheral circuitry and pitch circuitry formed on the die relative
12 to the memory arrays; the peripheral circuitry electrically interconnecting
13 with the pins and including operably interconnected control and timing
14 circuitry, address and redundancy circuitry, data and test path circuitry,
15 and voltage supply circuitry which collectively enable full access to all
16 addressable memory cells of the memory arrays.
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18 12. The semiconductor memory device of claim 11 wherein the
19 peripheral circuitry, the pitch circuitry, and the memory arrays are
20 fabricated to include a total of four or less composite conductive line
21 layers.
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1 13. The semiconductor memory device of claim 11 wherein the
2 peripheral circuitry, the pitch circuitry and the memory arrays have a
3 total combined continuous surface area on the die which is less than
4 or equal to 11.0 mm^2 .

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6 14. The semiconductor memory device of claim 11 wherein the
7 peripheral circuitry, the pitch circuitry, and the memory arrays are
8 fabricated to include at least five composite conductive line layers, the
9 occupied area of all functional and operable memory cells on the die
10 having a total combined area on the die which is no greater than
11 2.5 mm^2 .

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13 15. The semiconductor memory device of claim 11 wherein the
14 peripheral circuitry, the pitch circuitry, and the memory arrays are
15 fabricated to include at least five composite conductive line layers; the
16 peripheral circuitry, the pitch circuitry and the memory arrays having a
17 total combined continuous surface area on the die which is less than
18 or equal to 10.2 mm^2 .

1 16. A semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package
3 having an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;
5 a total of no more than 68,000,000 functional and operably
6 addressable memory cells arranged in multiple memory arrays formed on
7 the die, at least one of the memory arrays containing at least 100
8 square microns of continuous die surface area having at least 128 of
9 the functional and operably addressable memory cells; and
10 peripheral circuitry and pitch circuitry formed on the die relative
11 to the memory arrays; the peripheral circuitry electrically interconnecting
12 with the pins and including operably interconnected control and timing
13 circuitry, address and redundancy circuitry, data and test path circuitry,
14 and voltage supply circuitry which collectively enable full access to all
15 addressable memory cells of the memory arrays.

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17 17. The semiconductor memory device of claim 16 wherein at
18 least one of the memory arrays containing at least 100 square microns
19 of continuous die surface area having at least 170 of the functional and
20 operably addressable memory cells.

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1 18. A semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package
3 having an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;

5 a total of no more than 17,000,000 functional and operably
6 addressable memory cells arranged in multiple memory arrays formed on
7 the die, at least one of the memory arrays containing at least 100
8 square microns of continuous die surface area having at least 128 of
9 the functional and operably addressable memory cells; and

10 peripheral circuitry and pitch circuitry formed on the die relative
11 to the memory arrays; the peripheral circuitry electrically interconnecting
12 with the pins and including operably interconnected control and timing
13 circuitry, address and redundancy circuitry, data and test path circuitry,
14 and voltage supply circuitry which collectively enable full access to all
15 addressable memory cells of the memory arrays.

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17 19. The semiconductor memory device of claim 18 wherein at
18 least one of the memory arrays containing at least 100 square microns
19 of continuous die surface area having at least 170 of the functional and
20 operably addressable memory cells.

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1 20. A semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package
3 having an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;
5 a total of no more than 4,500,000 functional and operably
6 addressable memory cells arranged in multiple memory arrays formed on
7 the die, at least one of the memory arrays containing at least 100
8 square microns of continuous die surface area having at least 128 of
9 the functional and operably addressable memory cells; and
10 peripheral circuitry and pitch circuitry formed on the die relative
11 to the memory arrays; the peripheral circuitry electrically interconnecting
12 with the pins and including operably interconnected control and timing
13 circuitry, address and redundancy circuitry, data and test path circuitry,
14 and voltage supply circuitry which collectively enable full access to all
15 addressable memory cells of the memory arrays.

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17 21. The semiconductor memory device of claim 20 wherein at
18 least one of the memory arrays containing at least 100 square microns
19 of continuous die surface area having at least 128 of the functional and
20 operably addressable memory cells.

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1 22. A semiconductor memory device comprising:
2 a total of no more than 68,000,000 functional and operably
3 addressable memory cells arranged in multiple memory arrays formed on
4 a semiconductor die; and

5 circuitry formed on the semiconductor die permitting data to be
6 written to and read from one or more of the memory cells, at least
7 one of the memory arrays containing at least 100 square microns of
8 continuous die surface area having at least 128 of the functional and
9 operably addressable memory cells.

10 23. The semiconductor memory device of claim ⁹22 wherein the
11 total number of functional and operably addressable memory cells on
12 the semiconductor die is no more than 17,000,000.

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15 24. The semiconductor memory device of claim 22 wherein the
16 total number of functional and operably addressable memory cells on
17 the semiconductor die is no more than 4,500,000.

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19 25. The semiconductor memory device of claim 22 wherein at
20 least one of the memory arrays containing at least 100 square microns
21 of continuous die surface area having at least 170 of the functional and
22 operably addressable memory cells.

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1 26. The semiconductor memory device of claim 22 wherein at
2 least one of the memory arrays containing at least 100 square microns
3 of continuous die surface area having at least 170 of the functional and
4 operably addressable memory cells, and the total number of functional
5 and operably addressable memory cells on the semiconductor die is no
6 more than 17,000,000.

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8 27. The semiconductor memory device of claim 22 wherein at
9 least one of the memory arrays containing at least 100 square microns
10 of continuous die surface area having at least 170 of the functional and
11 operably addressable memory cells, and the total number of functional
12 and operably addressable memory cells on the semiconductor die is no
13 more than 4,500,000.
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